Short Papers

A Bond-Wire Inductor-MOS Varactor VCO Tunable From 1.8 to 2.4 GHz

Francesco Svelto and Rinaldo Castello

***Abstract*—This paper presents a technique that optimizes LC-tank CMOS voltage-controlled oscillators (VCOs) by minimizing the product of phase noise and power consumption. Moreover, it shows that the minimum depends on the tank's quality factor Q, the device noise coefficient γ, and the ratio between the maximum oscillation amplitude and supply voltage α. Prototypes, realized in a 0.35-μm process, show the following performances: −122.5 dBc/Hz at 600 kHz from a 1.9-GHz carrier, with 2-V supply voltage and 1-mA current consumption. The VCO can be tuned between 1.8–2.4 GHz, when the varactor control voltage is varied between 0–3.5 V. In the proposed realization, the tank is made of a metal–oxide–silicon varactor (operated between accumulation and deep depletion) and a bond-wire inductor, realized connecting two pads to a package frame lead to be compatible with the production environment.**

***Index Terms*—CMOS integrated circuits, LC oscillators, phase noise, radio frequency, varactors, voltage-controlled oscillators.**

I. Introduction

Deep-submicrometer CMOS processes typically achieve f_T in excess of 50 GHz, making them a serious alternative for low-noise RF circuits operating in the gigahertz range. Moreover, PMOS devices in scaled technologies are improving even faster than NMOS ones, potentially making CMOS the only complementary technology for RF applications. Examples of fully integrated CMOS front-ends employing only few external components have been given [1]–[3]. Nonetheless, a debate is still ongoing on whether CMOS will be limited to less stringent wireless applications or it will compete with multichip solutions even in the most stringent cell-phones arena. The realization of a highly integrated transceiver remains the ultimate goal of CMOS RF designers with some big challenges still to be overcome, e.g., rejection of large spurious signals, which might overwhelm highly sensitive blocks, feasibility of on-chip electronic tuning to compensate spreads due to process variations, etc. However, an unambiguous comparison between the achievable performances of single RF blocks, when realized in different technologies, has also to be established.

In a voltage-controlled oscillator (VCO), there is a tradeoff between its key parameters i.e., phase noise, power consumption, and frequency-tuning range [4]–[6]. In fact, to achieve low-phase noise, the oscillation amplitudes must be maximized. This means either increasing the biasing current or the tank inductance (assuming a given tank quality factor). The former increases the power consumption, the latter reduces the frequency tuning range (the tank capacitance is lowered and the fixed capacitive parasitic represent a higher fraction of the total).

In this paper, we propose a CMOS LC VCO designed to give the best possible compromise among the above contrasting requirements. The tank, used in the oscillator, is made up of bond-wire inductors and MOS varactors, operated between accumulation and deep depletion. Up to date, bond-wire inductors had not been used in large-volume production, due to concerns about their reproducibility. Very recently, however, a triple-band CMOS transceiver chip set employing bond-wire inductors in the RF VCO has been launched on the market [7]. The main advantage of a bond-wire inductor is its high quality factor. On the other hand, the spread in the inductance has to be electronically compensated, meaning that the varactor has to provide a large tuning range. A MOS varactor, operated between accumulation and deep depletion, has a tuning range large enough to fully compensate such a spread, while maintaining a high Q.

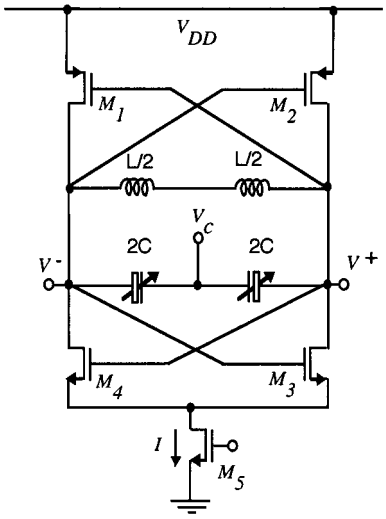

Fig. 1. Diagram of the LC CMOS VCO. Bond-wire inductors and MOS varactors realize the tank.

A prototype of the VCO described above was realized in a 0.35-μm CMOS process with the following performance: -122.5 dBc/Hz at 600 kHz from a 1.9-GHz carrier, while drawing 1 mA from a 2-V supply. The oscillation frequency can be varied between 1.8 –2.4 GHz, a tuning capability more than sufficient to compensate the expected $\pm 26\%$ variation in the values of the bond-wire inductance and of the varactor capacitance, once the design is centered. This level of performance places the proposed VCO very close to the best integrated oscillator ever reported [8]. Moreover, the present solution can further improve since the varactor quality factor (and, as a consequence, the tank quality factor) will benefit from scaling.

This paper is organized as follows. Section II shows how to minimize VCO phase noise leading to the optimum design. Sections III and IV present the design of the proposed VCO and the experimental results, respectively, and Section V draws the conclusions.

II. Phase-Noise Minimization

Fig. 1 shows the chosen LC CMOS VCO topology. To arrive at the guidelines for the optimum design, we use the Leeson's formula for the white phase noise $(\mathrm{PN}_W(\Delta\omega))$ at an offset frequency $\Delta\omega$ from an ω_0 carrier

$$\mathrm{PN}_W(\Delta\omega) = kTR\frac{F}{V_0^2}\left(\frac{\omega_0}{Q\Delta\omega}\right)^2 \quad (1)$$

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where k is the Boltzmann's constant, T is the absolute temperature, R is the equivalent tank parallel resistance, V_0 is the peak oscillation amplitude, Q is the tank quality factor. F, the noise factor, is given by [9]

$$F = 1 + \frac{4\gamma RI}{\pi V_0} + \gamma \frac{4}{9} g_{m\mathrm{bias}} R \tag{2}$$

where γ is the device white noise coefficient and $g_{m\mathrm{bias}}$ is the current source transconductance.

To compute V_0 notice that, at the peak of the oscillation, only one device of each pair (on opposite sides) is conducting, while the other is off. In this condition, all the core current (I) passes through the tank via the on devices. The tank current (I_{tank}) is, therefore, a square wave toggling between I and $-I$, and the peak oscillation amplitude is given by

$$V_0 = \frac{4}{\pi} RI = \frac{4}{\pi} \omega_0 LQI \tag{3}$$

in which $4/\pi I$ is the Fourier coefficient, at the fundamental frequency, of the tank current and $R = \omega_0 LQ$ at resonance.[1]

Increasing the bias current, (3) holds up to a current level (I_{SAT}) beyond which the oscillator amplitude ceases to increase. The value of I_{SAT} is given by

$$I_{\mathrm{sat}} = \frac{\pi}{4} \frac{1}{\omega_0 LQ} V_{\mathrm{sat}} \tag{4}$$

where V_{SAT} is the maximum oscillation amplitude.

Two regions of operation can then be identified, in which the oscillation amplitude is either dependent on the core current (current limited region) or saturates (voltage limited region). The phase noise has different dependence on the VCO parameters in the two regions [10].

If we notice that: 1) in the case of the chosen topology the noise contribution coming from the tail current [third term in (2)] can be made negligible with a small penalty on the value of V_{SAT} and 2) in the current limited region, the noise factor reduces to $1 + \gamma$, (1) can be written as follows:

$$\mathrm{PN}_W(\Delta\omega) = \begin{cases} kT \dfrac{1}{\omega_0 LQ^3} \dfrac{\pi^2(1+\gamma)}{16I^2} \left(\dfrac{\omega_0}{\Delta\omega}\right)^2 & \text{current limited} \\ kT \dfrac{\omega_0 L}{QV_{\mathrm{sat}}^2} \left(1 + \gamma \dfrac{4\omega_0 LQI}{\pi V_{\mathrm{sat}}}\right) \left(\dfrac{\omega_0}{\Delta\omega}\right)^2 & \text{voltage limited.} \end{cases} \tag{5}$$

Equation (5) shows that the phase noise decreases with current in the current-limited region and increases in the voltage-limited region. Therefore, minimum phase noise is achieved at the transition of the two regions, i.e., for $V_0 = V_{\mathrm{SAT}}$. Since V_{SAT} is primarily determined by the supply voltage, we can define α such that $V_{\mathrm{SAT}} = \alpha V_{DD}$. The optimum current (that gives the minimum phase noise) is given by $(\pi/4)(\alpha/\omega_0 LQ)V_{DD}$. As a consequence, the minimum phase noise is given by

$$\mathrm{PN}_W(\Delta\omega) = kT \frac{1}{Q^2} \frac{\pi(1+\gamma)}{4\alpha} \left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{V_{DD} I}. \tag{6}$$

From (6), the following important conclusions can be drawn: phase noise times power consumption depends only on γ, Q, and α at a given $\omega_0/\Delta\omega$.

[1]Due to finite switching time of transistors, at frequencies approaching the technology limit, the current through the tank might be better approximated by a sinusoid. In that case, $V_0 = \omega_0 LQI$.

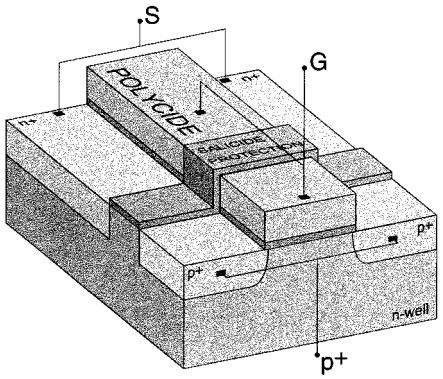

Fig. 2. Three-dimensional physical structure of the MOS varactor.

In scaled devices, γ can be in excess of 2/3 (its value in long channel devices) due to hot electron effects, and it can be considered a process parameter. The tank quality factor can be maximized by an optimal choice of inductor and varactor. Finally, α depends primarily on the topology and for the one proposed here is always less than one.

As a result, once the technology, oscillator topology, and tank quality factor are known, the optimum phase noise times power consumption of a VCO can be derived. Assuming α constant, notice that this optimum value is independent of the supply voltage or bias current, but depends only on their product.

To gain an intuitive insight in this result, let us consider the effect of a supply voltage change (e.g., due to the use of a different technology). If we assume the supply voltage is halved, so is V_{SAT}. If we decide to keep the power consumption constant, the bias current will have to be doubled. From (4), L will then be divided by four. As a consequence, both the output noise and signal power decrease by four, keeping the phase noise constant. On the other hand, if L is not changed, from (4), the bias current has to be halved. The power consumption is reduced by four, but the phase noise is increased by the same factor since the oscillation amplitude is halved.

Notice that, in the first case, i.e., supply voltage reduction with the same power consumption, the drawback is a tuning range reduction. In fact, while tank capacitance will increase by four, the parasitic capacitance associated with the cross-coupled transistors will increase substantially more than that. This is because the size of these transistors will have to increase to have one-half overdrive voltage (to keep α constant) with double bias current.

III. VCO Design

The combination of bond-wire inductors together with MOS varactors, proposed here, allows to achieve the highest tank quality factor, for the required tuning range, over other choices including spiral inductors and p-n varactors. In fact, spiral inductors feature a quality factor much lower than bond-wire inductors. On the other hand, a large varactor tuning range is required to compensate the larger spread of bond-wire inductors ($\pm 20\%$ of their nominal value). This could be accomplished by both MOS and p-n varactors. However to achieve such a high tuning range, p-n varactors need to be used in their forward bias region, resulting in a severe degradation of the tank quality factor.

The inductor is realized connecting two bond-wires between the output pads and a common frame lead. In this realization, a SO20 package is used and an estimate of the bond-wire length is 3 mm. Taking into account the mutual inductance of the two bond-wires, the overall tank inductance is estimated to be 6 nH. The varactor is an accumulation to a deep depletion-mode MOS varactor [11]. Fig. 2 shows the physical structure of the device. A p^+ region is created at the head of an N-MOS structure. n^+ and p^+ diffusions are housed in

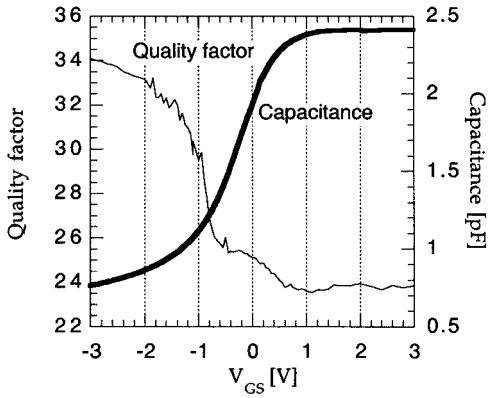

Fig. 3. Capacitance and quality factor for the accumulation to deep depletion-mode MOS varactor measured at 1.9 GHz.

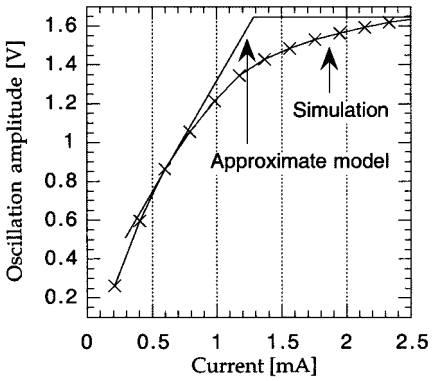

Fig. 4. Oscillation amplitude versus current, with a 2-V voltage supply at 1.9 GHz.

TABLE I
DESIGN SUMMARY

$(W/L)_{M1,M2}$	200/0.35	µm/µm
$(W/L)_{M3,M4}$	60/0.35	µm/µm
$(W/L)_{M5}$	400/1	µm/µm
I	1.1	mA
V_{DD}	2	V

the same n-well. For positive voltages applied between gate (terminal G) and source (terminal S), the surface layer is accumulated and the capacitance is maximum. When the applied voltage is reversed, a depletion region is formed underneath the gate. As the negative voltage is increased, the depletion region widens and the capacitance is reduced. When $V_{\rm GS}$ equals the device threshold voltage, an inversion layer would form. The reversely biased p^+-n-well junction removes the minority carriers from the inversion layer. As a result, the capacitance continues to decrease with increasing the reverse voltage applied between gate and source.

Fig. 3 shows the capacitance and quality factor versus the voltage applied between gate and source ($V_{\rm GS}$), measured at 1.9 GHz, for a realized prototype.

The minimum capacitance quality factor is 23. The bond-wire intrinsic quality factor is 50 at about 2 GHz. However, a few hundreds milliohms are sufficient to significantly reduce this value. Assuming

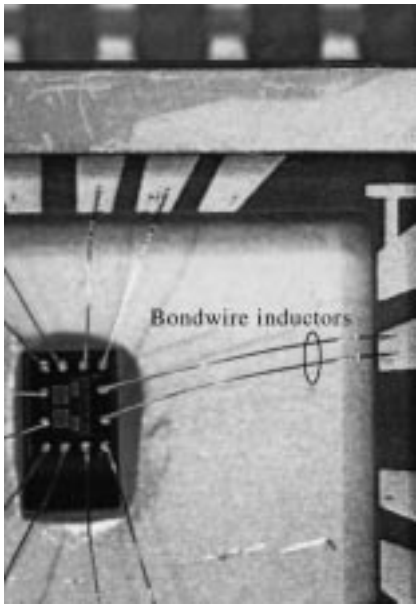

Fig. 5. Chip microphotograph.

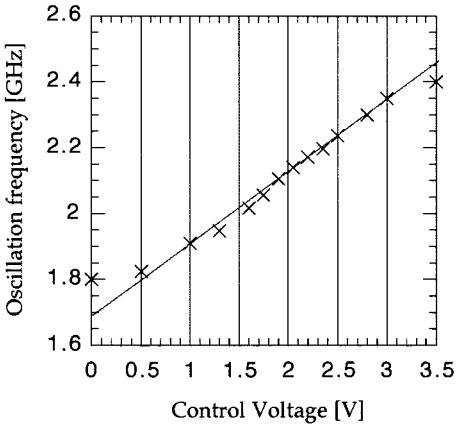

Fig. 6. Oscillation frequency versus control voltage.

600 mΩ for the parasitic resistance, the quality factor reduces to about 35. The expected Q of the tank is then 14. Knowing the inductance and tank quality factor, the optimum design can be carried on as follows.

- The active pairs are designed to have a low overdrive voltage, so as to maximize the saturation amplitude. Thus, the device width is only limited by the required capacitance tuning range (in this case, approximately $\pm 26\%$). Given the varactor capacitance tuning (shown in Fig. 3) and the bond-wire parasitic capacitance (primarily due to the capacitance of the pad), the n and p pairs aspect ratio is chosen to be 60/0.35 and 200/0.35 μm/μm, respectively.
- The optimum current value is derived based on Fig. 4, where the oscillation amplitude versus core current is shown. Both the approximate model, i.e., a linear region followed by saturation, and the result of a simulation performed at 1.9 GHz are reported. From the approximate model, the minimum phase noise times power consumption is obtained at the corner between the two regions (about 1.25 mA in the specific case). From simulations, the minimum is achieved for a 1.1-mA current. The difference is due to the inaccuracy of the approximate model at the edge of the linear region.

TABLE II
PERFORMANCE COMPARISON OF RECENTLY PUBLISHED VCOs

Ref.	Technology	I [mA]	V_{DD} [V]	PN [dBc/Hz]	FOM [dB]	Tuning range
[8]*	0.35μm CMOS	3.65	2.5	-152@3MHz from 1GHz	192.9	16%***
This work	0.35μm CMOS	1	2	-122.5@600kHz from 1.9GHz	189.5	28.5%
[8]**	0.35μm CMOS	3.65	2.5	-148.5@600kHz from 1GHz	189.4	NA
[13]	0.25μm CMOS	4.5	2.7	-128.5@600kHz from 2.1GHz	188.5	35%***
[14]	Bipolar	20	1.9	-148@3MHz from 1.5GHz	186.2	4.7%
[15]	0.5μm CMOS	1	3	-107@100kHz from 1.4GHz	185.1	17%

*Tail biased VCO
** Top biased VCO
***Discrete tuning

Finally, the resulting small-signal loop gain, equal to $g_m R$, with g_m being the small signal transconductance and R being the tank equivalent parallel resistance, must be sufficiently high to insure oscillation startup with a safe margin. In this case, $g_m R$ is about three, which is more than adequate. Table I reports the design values.

IV. Experimental Results and Performance Comparison

The VCO has been realized in a 0.35-μm CMOS technology. Fig. 5 shows the chip microphotograph. As shown, standard bond-wires connecting die pads to package frame leads are used.

All the measurements have been performed with a 2-V supply voltage for the VCO. On the other hand, the control voltage of the varactor is varied between 0–3.5 V (the maximum value allowed by the used technology). The varactor third terminal (p+) is fixed and kept to ground. In this condition, the oscillation frequency varies between 1.8–2.4 GHz, as shown in Fig. 6. If we limit the usable range to the region where the f–V relation is approximately linear and, as a consequence, the VCO gain is constant, i.e., between 0.5–3 V, the frequency can be varied between 1.82–2.35 GHz. This means that the oscillation frequency tuning range is 25.5% around 2.1 GHz. A $\pm$25.5% variation of the L times C value can then be compensated. This is practically enough to compensate the spread of the used tank elements. Notice that the three terminals MOS varactor allows a wider frequency tuning range than the standard MOS one. In fact, above roughly 2-V control voltage, a VCO using a standard MOS varactor would achieve its maximum oscillation frequency (since the capacitance would be minimum), while the three terminals can be further tuned.

Fig. 7 shows the phase noise relative to 1.9-GHz carrier versus the offset frequency, with 1-mA biasing current. The $1/f$ phase noise corner is around 100 kHz. The phase noise at 600-kHz offset is -122.5 dBc/Hz.

Fig. 8 shows phase noise at 600 kHz from 1.9 GHz times power consumption versus bias current. The minimum value is almost constant in the range of 1–1.3 mA and equals -119.5 dBc/Hz$*$mW.

As shown above, when the VCO design is optimum, phase noise can be traded with power consumption. Realizations, using different technologies and topologies, can then be compared based on the following figure-of-merit (FOM) [12]:

$$\mathrm{FOM} = \frac{1}{\mathrm{PN}(\Delta\omega) * V_{DD} I} \left(\frac{\omega_0}{\Delta\omega}\right)^2. \quad (7)$$

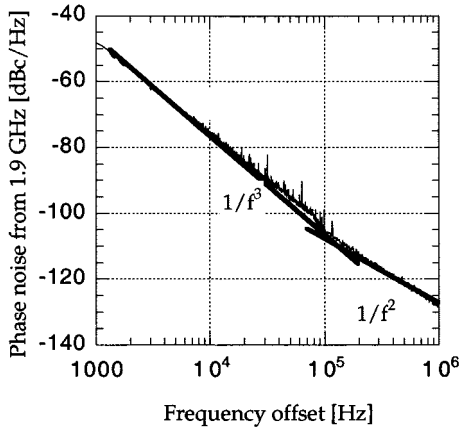

Fig. 7. Phase noise versus offset frequency from a 1.9-GHz carrier for I = 1 mA.

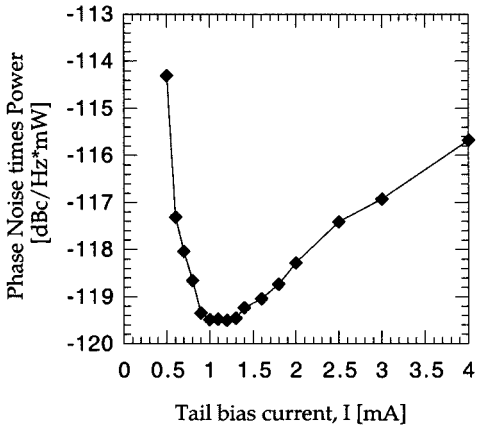

Fig. 8. Phase noise times power consumption at 600 kHz from a 1.9-GHz carrier versus bias current.

Table II gives the characteristic of recently published VCOs and compares the FOM and tuning range.

The higher four FOMs are achieved by CMOS realizations. The main reason for their superior performance is the larger oscillation amplitude, for given supply voltage, than bipolar solutions. The VCO of [8],

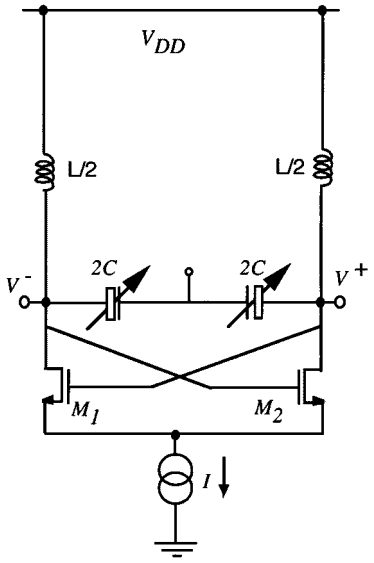

Fig. 9. Diagram of the LC CMOS VCO employing one cross-coupled pair.

based on the topology of Fig. 9, shows the highest FOM. Nonetheless, we still support the topology proposed here for the following reasons

- To achieve such a high FOM, the oscillation amplitude of the topology of Fig. 9 is well above the supply voltage (in principle, it can be twice as much). This means that the supply voltage has to be kept lower than the maximum value allowed by the technology and the oscillation amplitude must be limited to guarantee process reliability.
- The noise contribution of the tail current source transistor is intrinsically smaller in this topology (one-half everything else being the same) since the same oscillation amplitude is achieved with one-half the biasing current.

In addition, the MOS varactor Q will benefit from scaling. As a consequence, the quality factor of a tank using bond-wire inductors and the proposed MOS varactor will improve in further scaled technologies since the varactor limits the achievable Q.

V. Conclusions

This paper has provided the guidelines for the optimization of a CMOS LC VCO in terms of phase noise times power consumption, i.e., the actual parameter of interest. Equation (6) represents its theoretical minimum. Optimized CMOS VCOs compare favorably with their bipolar counterparts. To achieve very low FOM in future scaled technologies, tanks realized by means of bond-wire inductors are very attractive.

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Interface Loss Mechanism of Millimeter-Wave Coplanar Waveguides on Silicon

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***Abstract*—The interface loss mechanisms of coplanar waveguides (CPWs) on silicon with an SiO_2 isolation layer are investigated. The total losses of straight CPW lines of 7.5-mm length are measured between 45 MHz and 40 GHz and the interface contribution is extracted from that by its bias dependence. The interface losses depend on bias voltage and on the oxide quality. With an optimal bias voltage, the attenuation of a CPW with an unpatterned oxide layer always achieves a minimum. With bias between the flat-band voltage V_{FB} and threshold voltage V_{T} (depletion region), the interface losses are negligible. For high quality oxides (V_{T} around 0 V), very low attenuation was obtained without any bias.**

***Index Terms*—Bias-dependent attenuation, coplanar waveguide, depletion, interface losses, oxide, silicon, threshold voltage.**

I. Introduction

Low-doped silicon ($<10^{13}$ charge carriers per cm^3) is a suitable semiconductor substrate for low-loss microwave applications [1], [2]. The low-doped silicon is usually manufactured by a highly pure float

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